UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,317	12/18/2001	Fumihiko Hayakawa	1448.1018	8210

21171 7590 11/18/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,317	HAYAKAWA ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information Disclosure Statement(s) received 31 December 2003 has been considered. Please see attached PTO-1449(s).

Drawings

3. The drawings filed on 18 December 2001 have been approved by the Examiner.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell (US 5,014,195) in view of Albonesi (David H. Albonesi, "Selective Cache Ways: On-Demand Cache Resource Allocation," 1999).

As in claim 1, Farrell teaches:

a tag memory comprising n sections (Fig. 2, element 34; column 4, lines 30-35);

a cache memory comprising n sections (Fig. 2, element 42; column 4, lines 30-35);

a control unit which controls the switching of a way configuration to either an n-way configuration, in which all the cache memory sections are activated based on a configuration (i.e. mode) signal, or a 1-way configuration in which only one of the cache memory sections is active based on a value of an input request address (Fig. 1, element 12; column 4, lines 24-29; column 7, lines 18-37);

a data selector which selects only data read from any one of the cache memory section when reading the data (Fig. 2, element 44; column 4, lines 30-35; column 5, lines 44-56); and

a data selector control unit which controls the data selector so as to select only data read from the cache memory section corresponding to the value of a request address in case of the n-way configuration, and to select only data read from the one cache memory section in case of the 1-way configuration (Figs. 2 and 3, element 38; column 6, line 45 to column 7, line 37).

Farrell does not teach that the control unit is a power control unit such that the inactive cache memory sections are turned into a low power state as required by claim 1.

Albonesi teaches a power control unit for a cache memory where inactive sections of the cache memory are turned into a low power state in order to conserve power (Fig. 1; Abstract; § 2 and 3.1).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to have the control unit in Farrell, turn inactive cache memory sections into a low power state as taught by Albonesi, in order to conserve power as taught by Albonesi.

As in claim 2, Farrell teaches that the active cache memory sections are determined by logic based on the value of the request address and a value of the mode signal (Column 7, lines 18-37).

As in claim 3, Farrell teaches a tag determination circuit to determine if the address data read from each tag memory section is coincident with the value of the request address (Fig. 2, element 36; column 4, lines 30-35), and a data selector control circuit that selects any one of data read from each of the cache memory sections based on the determination result and a value of the mode signal, which is a control content of the control unit (Fig. 2, element 38; column 6, line 45 to column 7, line 37).

As to claim 4, although neither Farrell nor Albonesi explicitly teaches that the cache memory sections are divided from one module, such integration is well known in the art and

would have been obvious in the system of Farrell and Albonesi in order to obtain the advantages of increased integration, such as reduced pins and power consumption.

Claim 5 is rejected using the same rationale as for the rejection of claim 1 above, further noting that Albonesi teaches that the tag memory sections may also be selectively enabled (§ 3).

Claim 6 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 7 is rejected using the same rationale as for the rejection of claim 3 above.

Claim 8 is rejected using the same rationale as for the rejection of claim 3 above, where it is further noted that in Farrell the inactive tag sections participate in the tag comparison corresponding to a request address, and a hit result from an inactive section is invalidated by masking it's propagation using logical AND gates (Fig. 3, elements 60-62, 65-67, 70-72 and 75-77; column 6, line 63 to column 7, line 37).

Claims 9 and 10 are rejected using the same rationale as for the rejection of claim 4 above.

Claim 11 is rejected using the same rationale as for the rejection of claim 1 above, further noting that the tag memory sections of Farrell are connected in parallel (Fig. 2).

Claim 15 is rejected using the same rationale as for the rejection of claim 1 above.

Claims 12 and 16 are rejected using the same rationale as for the rejection of claim 2 above.

Claims 13 and 17 are rejected using the same rationale as for the rejection of claim 3 above.

Claims 14, 19 and 20 are rejected using the same rationale as for the rejection of claim 4 above.

Claim 18 is rejected using the same rationale as for the rejection of claim 8 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (571) 272-4212. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

Mano Padmanabhan
11/15/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER